



ON Semiconductor®

<http://onsemi.com>

LV5636VH

Bi-CMOS Integrated Circuit DC/DC converter for BS/CS antennas

Overview

LV5636VH integrates 1ch DC/DC boost converter and 1ch LDO. It is suitable as the power supply for BS/CS antennas of LCD/PDP TV and BD recorders that require automatic recovery without IC destruction and malfunction when the output is short-circuited.

Functions

DC/DC boost converter

- Soft-start time: 2.6ms
- Pulse by pulse over-current limiter

LDO

- Over-current limiter (Fold back)

ALL

- Under-voltage lockout
- Power good
- Output voltage setting resistor

- Frequency 1MHz operation
- Short circuit protector (constant timer: 1.6ms)

- Thermal shut-down protector
- Power good delay function
- Output voltage switching function (BS/CS)

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} maximum supply voltage	$V_{CC\ max}$		-0.3 to 25	V
LDOIN maximum input voltage	$V_{LDOIN\ max}$		-0.3 to 30	V
SW maximum voltage	$V_{SW\ max}$		-0.3 to 30	V
Allowable power dissipation	$P_d\ max$	*1	1.45	W
Operating temperature	T_{opr}		-30 to 85	$^\circ\text{C}$
Operating junction temperature	T_{jopr}		-30 to 125	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to 150	$^\circ\text{C}$

*1: When mounted on the specified printed circuit board (32.0mm × 38.0mm × 1.6mm), glass epoxy, double sides board

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LV5636VH

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V _{CC} supply voltage	V _{CC}		8 to 23	V
LDOIN input voltage	V _{LDOIN}		8 to 28	V
SW voltage	V _{SW}		-0.3 to 28	V
EN voltage	V _{EN}		0 to 23	V

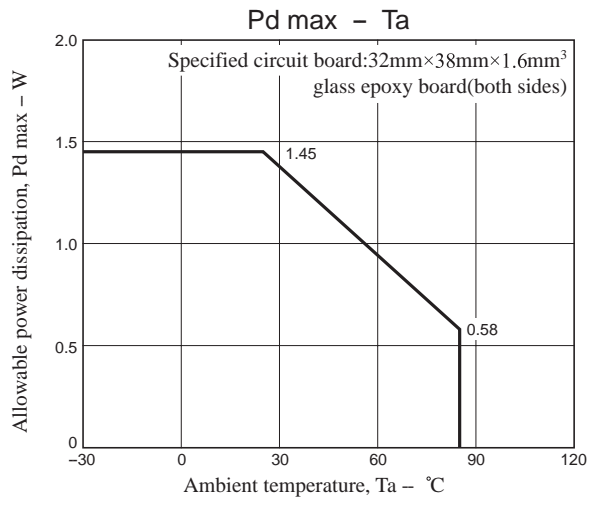
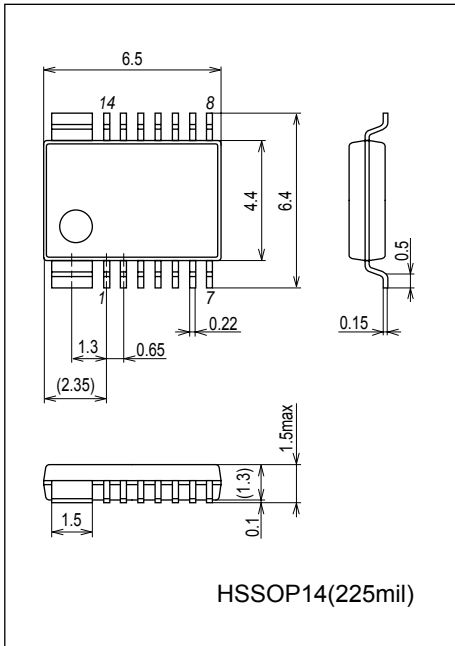
Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, V_{EN}=V_{CTL}=2V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
ALL						
Supply current	I _{CC}	Switching is turned off		2.1	4.0	mA
	I _{OFF}	EN=0V, LDOIN=0V			10	μA
Reference voltage	V _{REF}			1.26		V
LDO output voltage	LDOOUT1	CTL=High	(-2%)	15.9	(2%)	V
	LDOOUT2	CTL=Low	(-2%)	11.7	(2%)	V
DCDC output voltage	DCDCOUT1	CTL=High	(-2%)	16.5	(2%)	V
	DCDCOUT2	CTL=Low	(-2%)	12.3	(2%)	V
Enable voltage	V _{EN}		2.0			V
Disable voltage	V _{DIS}				0.4	V
EN input current	I _{EN}	V _{EN} =2.0V			10	μA
PGOOD threshold	V _{PG}	Power-good output is "good" when LDO is 85% or higher of the setting value.		85		%
PGOOD sink current	I _{PG}	Where power-good output is "no good" and V _{PGOOD} =0.5V.		1.0		mA
PGOOD leak current	I _{PGLK}	Where power-good output is "good" and V _{PGOOD} =2V			10	μA
PGDLY source current	I _{PGDLY}		3.84	4.8	5.76	μA
PGDLY threshold	V _{PGDLY}			1.26		V
CTL high voltage	V _{CTLH}	15V output setting	2.0			V
CTL low voltage	V _{CTLL}	11V output setting			0.4	V
CTL input current	I _{CTL}	V _{CTL} =2V			20	μA
UVLO on voltage	V _{UVLO}			7.0		V
Thermal shutdown temperature	TTSD	*2		155		°C
TSD hysteresis	THYS	*2		30		°C
DC/DC boost converter						
FB output voltage "Low"	FB low	I _N =2.0V, I _{FB} =-20μA (sink)			0.2	V
FB output voltage "High"	HB high	I _N =2.0V, I _{FB} =20μA (source)	1.8			V
Soft-start time	T _{SS}			2.6		ms
Oscillator frequency	f _{OSC}			1		MHz
Max ON duty	D max			85		%
SW ON resistance	R _{ON}			0.7		Ω
SW peak current	I _{PK}			1.8		A
SCP timer	t _{SCP}			1.6		ms
LDO						
Maximum output current	I _{O max}		450	620	800	mA
Line regulation	R _{LN}	16.5V < LDOIN < 21.5V			20	mV
Load regulation	R _{LD}	10mA < I _O < 300mA			50	mV
Dropout voltage	V _{DROP}	I _O =400mA		0.35	0.5	V
Short current	I _{SHORT}	LDOOUT=GND			100	mA

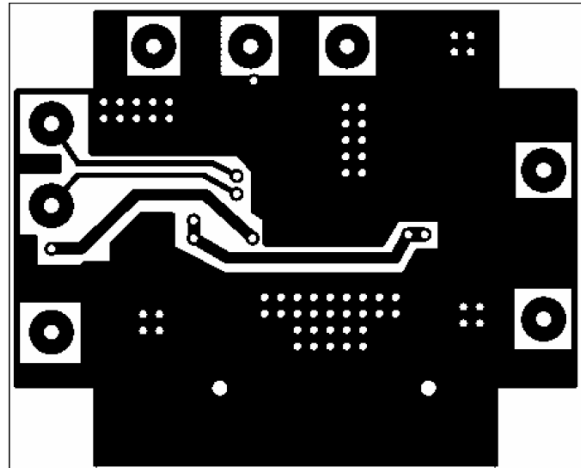
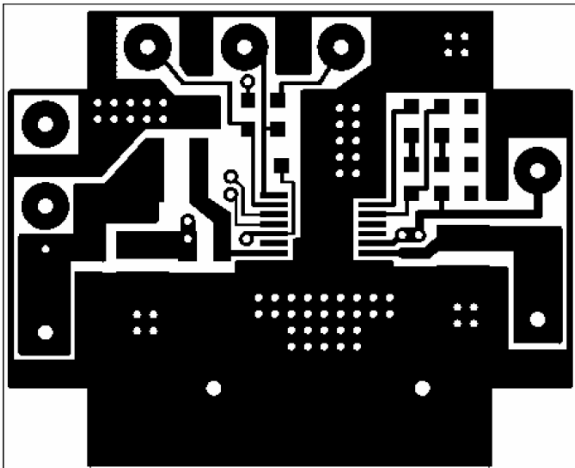
*2: Design guarantee value.

Package Dimensions

unit : mm (typ)
3313

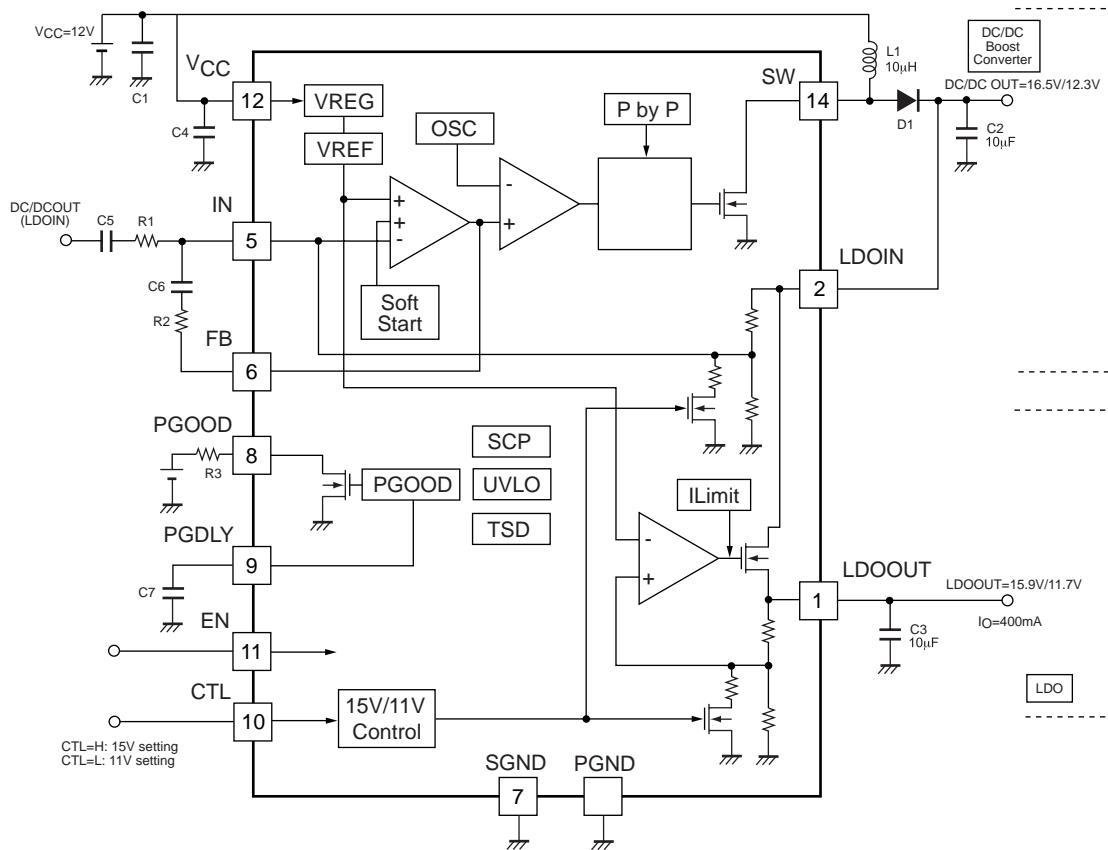


Specified board (32mm×38mm×1.6mm, glass epoxy, double side board)



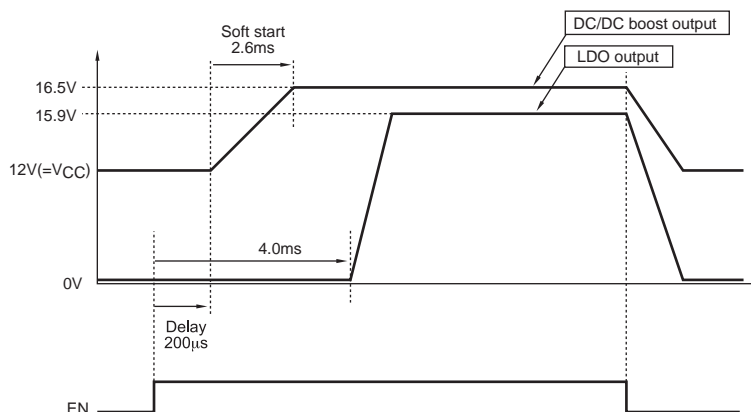
LV5636VH

Block diagram and Application circuit



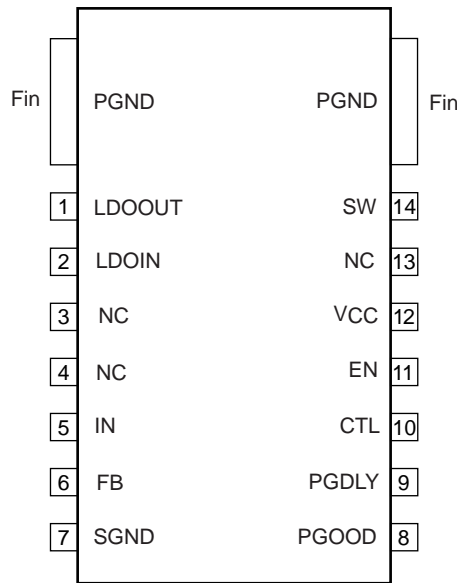
Start and stop

Output waveform during start and stop is shown below.



LV5636VH

Pin arrangement



Top view

Pin function

Pin No.	Pin name	Function	Equivalent circuit
1 2 7	LDOOUT LDOIN SGND	LDO output LDO input Signal ground	
5	IN	DC/DC error amplifier input	
6	FB	DC/DC error amplifier output	
8	PGOOD	Power good output	

Continued on next page.

LV5636VH

Continued from preceding page.

Pin No.	Pin name	Function	Equivalent circuit
9	PGDLY	PGDLY capacitor connection pin for delay time setting	
10	CTL	15V, 11V output voltage switching	
11 12	EN VCC	Enable Power supply	
14 Fin	SW PGND	DC/DC open drain output Power ground	

Function overview

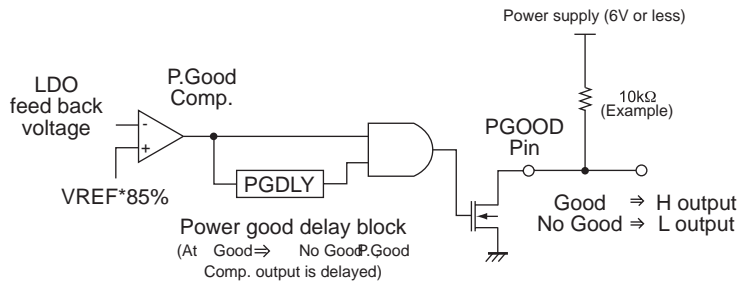
(1) UVLO (Under Voltage Lockout)

UVLO stops outputs of both DC/DC and to LDO to prevent malfunction when V_{CC} decreases. UVLO operates when V_{CC} falls below the UVLO voltage. This function is a non-latch-type, and recovers these outputs automatically when V_{CC} exceeds the UVLO voltage.

(2) Power good

Power good notifies that the output voltage of LDO is within the range of the setting voltage. The output is judged to be “power good” when both outputs are 85% or higher compared to the setting voltages. If the output voltage falls below 85%, PGOOD output becomes H→L (No Good). At “Good”→”No Good”, delay time can be set. It explains this at (3). When EN=L (OFF), PGOOD output is H.

[Power good circuit diagram]

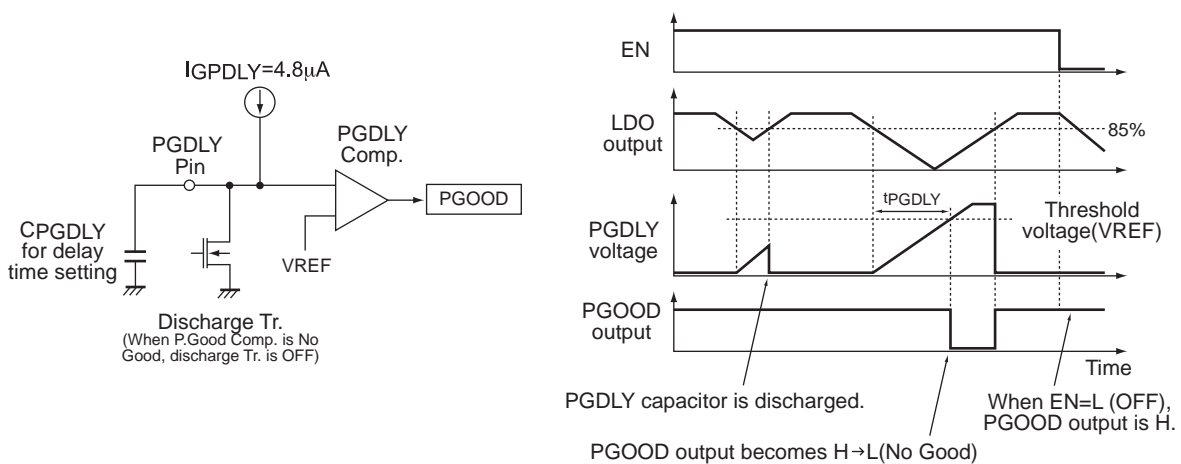


(3) Power good delay

If the output voltage of LDO falls below 85%, charge at $4.8\mu\text{A}$ constant starts to PGDLY capacitor for delay time setting. When PGDLY voltage exceeds the threshold voltage (=VREF), PGOOD voltage reaches to the threshold voltage, PGDLY capacitor using the following formula because delay time (t_{PGDLY}) depends on capacitance.

$$C_{PGDLY} = (I_{PGDLY} \times t_{PGDLY}) / V_{REF}$$

[PGDLY circuit diagram]

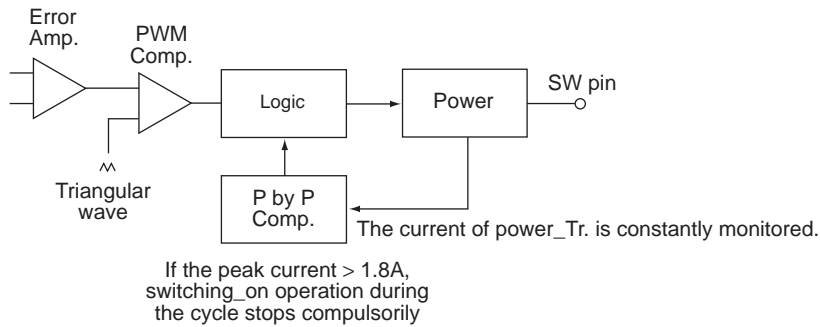


LV5636VH

(4) Pulse-by-Pulse over current protection (P by P)

The P by P stops switch-on operation of a certain cycle by force when the current of power MOSFET reaches the maximum output peak current.

[P by P circuit diagram]



(5) Short circuit protector (SCP)

When output voltage of DC/DC decreases due to short-circuit; for example, SCP latches off the outputs of DC/DC and LDO by timer.

When output voltage of DC/DC decreases and FB that is the error amplifier output turns to H, the internal counter starts, latch-off occurs after 1.6ms.

To restart the output after latch-off, you need to input EN signal again.

(6) Output voltage switching function

Where CTL=High, 15V output setting is selected.

Where CTL=Low, 11V output setting is selected.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.